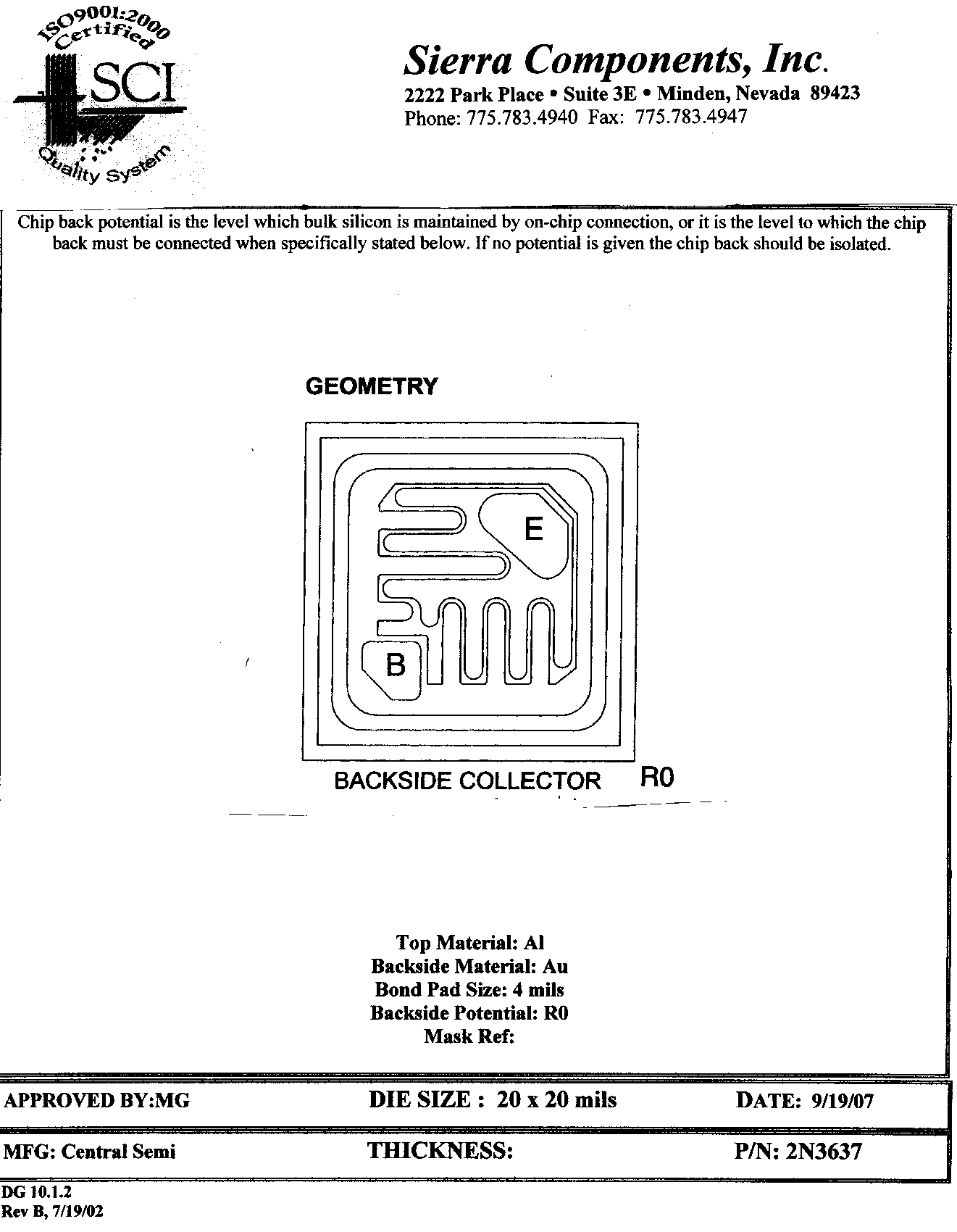
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.020”**

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**.020”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004” min.**

**Backside Potential: COLLECTOR**

**Mask Ref: CP716**

**APPROVED BY: DK DIE SIZE .020” X .020” DATE: 10/7/21**

**MFG: CENTRAL SEMI THICKNESS .009” P/N: 2N3637**

**DG 10.1.2**

#### Rev B, 7/1